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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/651,523	08/29/2003	Steven K. Reinhardt	42P15451	8550

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EXAMINER	
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ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/651,523	REINHARDT ET AL.	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This Office Action is in response to the application 10/651,523 filed on 08/29/2003.

2. Claims 1-27 are again presented for examination.

3. The Applicant is suggested to update the specification, page 2, the Attorney docket numbers with the application serial numbers.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the

art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bossen et al. (U.S. 6,058,491 hereafter referred to as Bossen) in view of Fleming et al. (U.S. 6,023,772 hereafter referred to as Fleming).

As per claim 1:

Bossen substantially teach the invention. Bossen teaches:

- A method comprising:

- storing an architectural state of a processor corresponding to a first checkpoint [fig. 3, col. 3, lines 20-30; col. 5, lines 50-58];
- determining whether an processing error has occurred subsequent to the storage of the first checkpoint [col. 2, lines 1-4; col. 3, lines 20-30; and col. 8, lines 25-45];
- restoring the architectural state of the processor corresponding to the first checkpoint [fig. 3, col. 3, lines 20-30; col. 5, lines 50-58].

Bossen does not explicitly address:
- non-deterministic events.

However, Bossen does disclose capability of:
- A method and system for fault handling to improve reliability of a data processing system having leading and lagging processes via computing processing [abstract, fig. 3, col. 1, lines 1-12 and col. 3, lines 30 through col. 4, line 10] comprising:
- a data connectivity among processors, instruction memory, data memory, I/O interfaces, etc… [fig. 1-3, col. 2, lines 50 through col. 3, line30].

- ***a fault/error detection and correction processes via processing loading operation, executing, timing, retrying, synchronizing, checkpointing, state information retrieval, comparison, resetting, re-executing operations, etc…(i.e., non-deterministic events and/or failure behaviors***) in supporting the fault-tolerant/ hardware failure and recovery process [fig. 3, col. 3, lines 20-30; col. 5, lines 50-58; col. 5, lines 60-67; col. 6, lines 63-67; col. 7, lines 19-60].

In addition, Fleming explicitly teaches:

- A fault-tolerant processing system including multiple processors and checkpointing techniques [abstract, fig. 2, col. 1, lines 1-10] comprising:
- a checkpointing the state information and securely storing non-determinstic event information in supporting the fault-tolerant process [col. 2, lines 44-64].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Bossen's ***fault/error detection and correction processes via processing loading operation, executing, timing, retrying, synchronizing, checkpointing, state information***

retrieval, comparison, resetting, re-executing operations, ***etc...(i.e., non-deterministic events and/or failure behaviors***) in supporting the fault-tolerant/ hardware failure and recovery process as being the ***non-deterministic events*** as claimed by Applicant. This is because Bossen's data/fault tolerant system explicitly performed data failure detection and recovery via state information (i.e., architectural state), checkpointing, storing, and executing process. By utilizing these capabilities, the computer hardware system can be directed or redirected promptly and functioned properly during failure process in supporting the network operation via its non-deterministic event function determination; second, by applying the ***checkpointing the state information and securely storing non-determinstic event information in supporting the fault-tolerant process*** as taught by Fleming in conjunction with the method and system for fault handling to improve reliability of a data processing system having leading and lagging processes via computing processing as taught by Bossen, the computing operation process within fault tolerant networking system including re-executing capability (i.e., error detection and correction) can enhance its operation performance, more specifically to ensuring the error detected, corrected, and replaced (i.e., backup) in proper and efficient manner via its checkpointing functionality.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the fault-tolerant system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

As per claims 2-4:

Bossen further teaches:

- synchronizing a leading thread of instructions and a trailing thread of instructions [col. 3, lines 1-30 and col. 7, lines 44-61].
- checking outputs from the leading thread of instructions and the trailing thread of instructions for faults [col. 7, lines 44-61].
- storing values from one or more architectural registers in a memory external to one or more processors executing the leading thread of instructions and the trailing thread of instructions [col. 3, lines 1-30 and col. 5, lines 50-58].

- wherein the leading thread of instructions and the trailing thread of instructions are executed [fig. 3, col. 3, lines 60 through col. 4, lines 10];

-- by a single processor [fig. 1, col.2, lines 55-66].

-- by multiple processors [fig. 1, col.2, lines 55-66].

In addition, Fleming explicitly teaches:

- A fault-tolerant processing system including multiple processors and checkpointing techniques [abstract, fig. 2, col. 1, lines 1-10] comprising:

- a checkpointing the state information and securely storing non-determinstic event information in supporting the fault-tolerant process [col. 2, lines 44-64].

- a fault tolerant connectivity among multiple processors, error detection and correction devices including failure behaviors[fig. 2, col. 6, lines 35-57; col. 9, lines 64 through col. 10, lines 15].

As per claims 5-6:

Bossen further teaches:

- selectively flushing (i.e., ***discard***) results of instructions that started execution after an instruction

causing the fault started execution [fig. 3, col. 24, lines 61-66; col. 5, lines 26-35 and col. 6, lines 7-21];

- restoring architectural state to a checkpoint corresponding to a state at which the instruction causing the fault started execution [fig. 3, col. 3, lines 20-30; col. 5, lines 50-58];

- re-executing instructions executed after the checkpoint to the instruction causing the fault using the logged non-deterministic events [fig. 3, col. 10, lines 18-47];

- discarding one or more outputs generated by the re-execution of the instructions executed after the checkpoint to the instruction causing the fault using the logged non-deterministic events [fig. 3, col. 24, lines 61-66; col. 5, lines 26-35 and col. 6, lines 7-21].

As per claims 7-9:

Bossen further teaches:

- continuing execution of instructions subsequent to the instruction causing the fault [fig. 3, col. 8, lines 25-45];

- wherein restoring architectural state to a checkpoint corresponding to a state at which the instruction causing

the fault started execution comprises [fig. 3, col. 3, lines 20-30; col. 5, lines 50-58];

-- restoring the architectural state to a state prior to execution of the instruction causing the fault [col. 8, lines 35-39];

-- restoring the architectural state to a state a the beginning of execution of the instruction causing the fault [col. 8, lines 35-39];

In addition, Fleming explicitly teaches:

- A fault-tolerant processing system including multiple processors and checkpointing techniques [abstract, fig. 2, col. 1, lines 1-10] comprising:

- a checkpointing the state information and securely storing non-determinstic event information in supporting the fault-tolerant process [col. 2, lines 44-64].

- a fault tolerant connectivity among multiple processors, error detection and correction devices including failure behaviors[fig. 2, col. 6, lines 35-57; col. 9, lines 64 through col. 10, lines 15].

As per claims 10-14:

Bossen further teaches:

- a load operation [col. 3, lines 47-50];

- a timing-dependent operation comprises a read operation of a cycle counter [col. 3, lines 12-18; col. 7, lines 33-43; col. 9, lines 3-55];

Bossen does not explicitly address:

- the non-deterministic event comprises an asynchronous interrupt.

However, Bossen does disclose capability of:

- A method and system for fault handling to improve reliability of a data processing system having leading and lagging processes via computing processing [abstract, fig. 3, col. 1, lines 1-12 and col. 3, lines 30 through col. 4, line 10] comprising:

- a data connectivity among processors, instruction memory, data memory, I/O interfaces, etc… [fig. 1-3, col. 2, lines 50 through col. 3, line30].

- ***a fault/error detection and correction processes via processing loading operation, executing, timing, retrying, synchronizing, checkpointing, state information retrieval, comparison, resetting, re-executing operations, etc…(i.e., non-deterministic events and/or failure behaviors; and/or***

interrupt) in supporting the fault-tolerant/ hardware failure and recovery process [fig. 3, col. 3, lines 20-30; col. 5, lines 50-58; col. 5, lines 60-67; col. 6, lines 63-67; col. 7, lines 19-60].

In addition, Fleming explicitly teaches:

- A fault-tolerant processing system including multiple processors and checkpointing techniques [abstract, fig. 2, col. 1, lines 1-10] comprising:
- a checkpointing the state information and securely storing non-determinstic event information in supporting the fault-tolerant process [col. 2, lines 44-64].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Bossen's ***fault/error detection and correction processes via processing loading operation, executing, timing, retrying, synchronizing, checkpointing, state information retrieval, comparison, resetting, re-executing operations, etc…(i.e., non-deterministic events and/or failure behaviors; and/or interrupt***) in supporting the fault-tolerant/ hardware failure and recovery process as being the ***non-deterministic event comprises an asynchronous interrupt*** as claimed by

Applicant. This is because Bossen's data/fault tolerant system explicitly performed data failure detection and recovery via state information (i.e., architectural state), checkpointing, storing, and executing process. By utilizing these capabilities, the computer hardware system can be directed or redirected promptly and functioned properly during failure process in supporting the network operation via its non-deterministic event function determination; second, by applying the ***checkpointing the state information and securely storing non-determinstic event information in supporting the fault-tolerant process*** as taught by Fleming in conjunction with the method and system for fault handling to improve reliability of a data processing system having leading and lagging processes via computing processing as taught by Bossen, the computing operation process within fault tolerant networking system including re-executing capability (i.e., error detection and correction) can enhance its operation performance, more specifically to ensuring the error detected, corrected, and replaced (i.e., backup) in proper and efficient manner via its checkpointing functionality for the same reasons set forth as described in claim 1, **supra**.

As per claims 15-17:

Due to the similarity of claims 15-17 to claims 1-14 except for an ***apparatus*** comprising ***means*** for storing an architectural state of a processor, ***means*** for storing non-deterministic events, ***means*** for determining whether an processing error has occurred, ***means*** for restoring the architectural state of the processor, etc… instead of a ***method*** comprising storing an architectural state of a processor, storing non-deterministic events, determining whether an processing error has occurred, restoring the architectural state of the processor, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-14. **In addition, all of the limitations have been noted in the rejection as per claims** 1-14.

As per claims 18-22:

These claims are similar to claims 1-14; the only the minor different is that these claims address "a load value queue" stored in memory. However;

Bossen further teaches:

- leading/trailing thread execution circuitry (i.e., leading and lagging processors) [fig. 1-3, col. 2, lines 42-58].

- memory used in supporting the hardware failure detection and correction [col. 7, lines 19-43];

- ***computing operation value registers used in sequencing and ordering (i.e., value queuing) from memory or buffer for comparison leading and lagging processes*** [col. 6, lines 7-67];

In addition, Fleming explicitly teaches:

- A fault-tolerant processing system including multiple processors and checkpointing techniques [abstract, fig. 2, col. 1, lines 1-10] comprising:

- a checkpointing the state information and securely storing non-determinstic event information in supporting the fault-tolerant process [col. 2, lines 44-64].

- ***information/entities queuing and/or arrangement used to support fault-tolerant process*** [col. 4, lines 30-67; col. 5, lines 1-14].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of Applicant's invention to first realizing Bossen's ***computing operation value registers used in sequencing and ordering (i.e., value queuing) from memory or buffer for comparison leading and lagging processes*** in

supporting the fault-tolerant/ hardware failure and recovery process as being the ***value queue*** as claimed by Applicant. This is because Bossen's data/fault tolerant system explicitly performed data failure detection and recovery via state information (i.e., architectural state), checkpointing, storing, and executing process; Therefore, by utilizing this sequencing or ordering (i.e., value queuing) feature, information and checkpointing can be validated for its hardware error recovery and comparison process; second, by applying the ***information/entities queuing and/or arrangement used to support fault-tolerant process*** as taught by Fleming in conjunction with the method and system for fault handling to improve reliability of a data processing system having leading and lagging processes via computing processing as taught by Bossen, the computing operation process within fault tolerant networking system including re-executing capability (i.e., error detection and correction) can enhance its operation performance, via its checkpointing functionality.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the fault-tolerant system operation availability and network/system performance, data connectivity, data reliability.

As per claims 23-27:

Due to the similarity of claims 23-27 to claims 18-22 except for a ***system*** comprising leading thread execution circuitry, trailing thread execution circuitry, a memory, etc…; instead of the ***apparatus*** comprising leading thread execution circuitry, trailing thread execution circuitry, a memory, etc… therefore, these claims are also rejected under the same rationale applied against claims 18-22. **In addition, all of the limitations have been noted in the rejection as per claims** 18-22.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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